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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/730,453	12/05/2000	Paul C. Dorsey	ENB-004/(C0441/7147)	8461

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EXAMINER	
WILSON, ROBERT W	
ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 10/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/730,453	DORSEY ET AL.	
	Examiner	Art Unit	
	Robert W Wilson	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-33* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 May 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1.0 The application of Frazier et. al. entitled MULTI-PORTAL POCKET TRANSLATOR filed on 12/5/2000 and requesting priority based upon DIV 08/974,632 dated 11/19/1997 and amended on 5/30/01 was examined. Claims 1-33 are pending.

Claim Rejections - 35 USC § 103

2.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3.0 **Claims 1-3 & 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Seter et. al. (U.S. Patent No.; 5,651,002)

Referring to **Claim 1**, Van Seter teaches: A translator unit for translating a packet formatted according to a first protocol into a packet according to a second protocol (Interworking device between an Ethernet or first protocol and FDDI or second protocol per col. 1 line 15-col. 2 line 63)

An input memory (Memory in the receiving MAC per col. 1 lines 53-67)

At least one information source (Supplemental information is provided from by an information source when the disassembling and reassembling registers or memory provide supplemental information per col. 1 line 63-col. 2 line 24)

An output memory (Memory in transmitting MAC per col. 1 lines 53-67)

A connection circuit, coupled to the input memory, the information source and output memory to selectively connect the input memory and the information source to the output memory (control circuitry per col. 1 line 53-col. 1 line 25)

A microcoded control unit coupled to the connection circuit (Processor for packet manipulation which works in conjunction with the control circuitry per col. 1line 52-67)

Van Seter does not expressly call for: microcoding of the control unit but teaches a packet processor.

It is within the level of one skilled in the art at the time of the invention to implement the packet processor as a microcoded control unit.

In Addition Van Seter teaches:

Regarding **Claim 2**, wherein the information source is selected form the group consisting of a register, a FIFO memory, a random access memory and an opcode memory storing data as operands of microcoded instruction (RAM per col. 2 lines 49-63)

Regarding **Claim 3**, wherein the microcoded control unit includes a pipeline unit (The reference teaches that the processor controls disassembling and reassembling in registers in sequential steps. The examiner take official notice utilizing a pipeline processor to performing sequential steps involving registers is well known in the art to utilizing a pipeline processor per IBM Dictionary of Computing Pg 324.. It would have obvious to one or ordinary skill in the art at the time of the invention to utilize a pipeline processor in order to perform sequential manipulations of data in registers or memories)

Regarding **Claim 8**, further comprising a direct memory access controller coupled to the input memory and output memory (The applicant broadly claims direct "memory access controller". The examiner interprets that the processor directly access memory and therefore is a direct memory access controller.)

Claim Rejections - 35 USC § 103

4.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.0 **Claims 10 & 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroiwa et. al. (U.S. Patent No.; 5,809,552)

Referring to Claim 10, Kuroiwa teaches: A piplined control unit for reading data (Control Unit per Figs 1 & 2) comprising:

A first memory having a first read latency (Memory 5 per Fig 1. The examiner takes official notice that memories having different latencies are well known in the art per 5,787,255 col. 1 line 52-col. 2 line 39)

A second memory having a second read latency, longer than the first read latency (Memory 5 per Fig 1. The examiner takes official notice that memories having different latencies are well known in the art per U.S. Patent No.: 5,787,255 col. 1 line 52-col. 2 line 39)

A pipeline unit having a first stage and a second stage (The applicant broadly claims a first stage and a second stage. The examiner has interpreted a first stage and a second stage to mean a first prefetch address and a second prefetched address in a pipeline . The reference teaches a four stage pipeline is set up per Figure 4.)

A circuit, coupled to the pipeline unit the first memory and the second memory, to initiate read cycles from the first memory based on a first instruction in the second stage of the pipeline, and to initiate read cycles from the second memory based on a second instruction in the first stage of the pipeline (Bus and Control Unit per Figs 1 & 2 setting up a pipeline per Fig 4)

The reference does not expressly call for: read instruction from the first memory based on first instruction in the second stage of the pipeline and initiate read cycles from the second memory based on a second instruction in the first stage of the pipeline but teaches that central processing is utilized to access memory when the bus width of the device does not match the bus width per col. 18 lines 52-67 and memories which have different latencies are well known in the art per U.S. Patent No.: 5,787,255 col. 1 line 52-col. 2 line 39)

I t would have been obvious to one of ordinary skill in the art at the time of the invention to prefetch instructions in two stages in order to access memories which do not have a latency or access speed which matches the width of the bus. Since the latency of the first memory is shorter than the latency of the second memory, it would have been obvious to one of ordinary skill in the art at the time of the invention to store the memory access for the shorter latency in the first stage and the second memory access in the second stage.

In Addition: Kuroiwa teaches:

Regarding Claim 11, further comprising a microcontroller coupled to the circuit (control unit or microcontroller per Fig 1 & 2)

Claim Rejections - 35 USC § 103

6.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be

patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7.0 Claims 12 & 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deb et.

al. (U.S. Patent No.; 6,172,990)

Referring to **Claim 12**, Deb teaches: A method of translating an original packet from a first protocol to a second protocol (The applicant broadly claims "first protocol" and "second protocol" Translates Ethernet or first protocol to an intermediate form or second protocol by adding a data structure per Fig 3A, 2B, &4a or abstract) comprising the steps of:

Loading a first memory with a plurality of sets of microcode instructions, each set being designed to perform a different network communication protocol translation (Microcode for SNAP vs 802.3 is utilized to add a data structure per col. 12 lines 30-col. 13 line 23. The microcode is loaded in RAM 302 per Fig 3B or first memory)

Receiving the original packet (115 per Fig 3B)

Selecting a one of the sets of the sets of microcode instructions,based on the identity of the first protocol and the identify of the second protocol (Microcode for SNAP vs 802.3 is utilized to add a data structure per col. 12 lines 30-col. 13 line 23. The examiner has interpreted SNAP and 802.3 as the first protocol and the intermediate form with a data structure as the second protocol)

Translating the original packet into a translated packet by executing the selected set of microcode instructions (The original packet is translated from 802.3 or SNAP into an intermediate form with a data structure per Figures 2B and 3B and Figure 4A)

Deb does not expressly call for: a first protocol and a second protocol but teaches translation of 802.3 or SNAP or first protocols into an intermediate form that has a data structure.

It would have been obvious to one of ordinary skill in the art at the time of the invention that the intermediate form with a data structure forms the same function as a second protocol and Ethernet or SNAP perform the same function as a first protocol.

In Addition Deb teaches:

Regarding **Claim 11**, further comprising a micro-controller coupled to the circuit (micro-RISC stream process or micro-controller per col. 12 line 35)

Referring to **Claim 14**, Deb teaches: A method of translating an original packet into a translated packet (The applicant broadly claims translating an original packet into a translated packet. The reference teaches translating Ethernet or original packet into to an intermediate form or

translated packet by adding a data structure per Fig 3A, 2B, &4a or abstract) comprising the steps of:

Loading an instruction memory with a set of instructions (Microcode for SNAP vs 802.3 is utilized to add a data structure per col. 12 lines 30-col. 13 line 23. The microcode is loaded in RAM 302 per Fig 3B or instruction memory)

Providing an information source (316 per Fig 3B is an information source)

Providing an output memory to store the translated packet (108 per Fig 2B or memory)

Sequentially, selectively connecting the input memory and the information source to the output memory, based on the instructions (The received packet goes through a series of Pipeline Register stages sequentially per 323 per fig 3B wherein the input memory provides information which can be utilized to determine the Data Structure to be added per 316 per Fig 3B)

Deb does not expressly call for: translating an original packet into a translated packet but teaches translating Ethernet or SNAP into an intermediate form with a data structure.

It would have been obvious to one of ordinary skill in the art at the time of the invention that translating Ethernet or SNAP into an intermediate form with a data structure performs the same function as translating an original packet into a translated packet.

In Addition Deb teaches:

Regarding **Claim 15**, wherein the loading step comprises a step of loading microcoded instructions (RISC software instructions or microcode per col. 12 line 35)

Regarding **Claim 16,** wherein the connecting step comprises a step of feeding the instructions through a pipeline unit (The figures 3B and 2B define a series of sequential steps. The examiner takes official notice that pipeline processing is well known in the art to be utilized in applications that utilize sequential steps. It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize a pipeline unit to performs these sequential steps)

Claim Rejections - 35 USC § 103

8.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9.0 **Claim 27** is rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch (U.S. Patent No.; 4,025,771)

Referring to **Claim 27**, Lynch teaches: A pipelined control unit for reading data (Figure 1 comprising:

A first memory having a first latency (Main Memory or magnetic disk per Fig 1 and col. 3 lines 24-30. The examiner takes official notice that it is well known in the art that magnetic memory is slower than RAM per U.S. Patent No.: 5,253,360 per col. 1 lines 31-46. It would have been obvious to one of ordinary skill in the art at the time of the invention that magnetic disk would have a different latency from RAM .)

A second memory having a second latency (Input Memory per Fig 1 which is RAM per col. 3 lines 24-30. The examiner takes official notice that it is well known in the art that magnetic memory is slower than RAM per U.S. Patent No.: 5,253,360 per col. 1 line 31-46. It would have been obvious to one of ordinary skill in the art at the time of the invention that magnetic disk would have a different latency from RAM)

A pipeline unit having a first set of registers for processing an operand and a second set of registers for processing an opcode, the pipeline unit having a first stage and a second stage (Figure 1 or col. 4 lines 40-col. 6 line 10 discloses a pipeline unit having 7 stages)

A control circuit coupled to a first memory, the second memory , and the pipeline unit for initiating a read cycle in a first memory during the first stage and for initiating a read cycle in the second memory during the second stage (The applicant broadly claims a "first stage" and a "second stage". The examiner interprets a "first stage" as a step to read data from the Main Memory or Magnetic Disk and a "second stage" as a step to read from Input Memory or RAM per Fig 1)

Lynch does not expressly call for: a first stage and a second stage but teaches 7 stages.

It would have been obvious to one of ordinary skill in the art at the time of the invention to scale the number of stages to the number of devices which are read or from 7 to 2.

Claim Rejections - 35 USC § 112

10.0 The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11.0 Claims 4-5, 10-11, 17-18, & 20-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Referring to **Claims 4**, the applicant refers two "two pipelines"? What is meant by "two pipelines"? Does the applicant mean two processors or does the applicant mean two pipeline queues?

Referring to **Claims 6**, the applicant refers to "four pipelines"? What is meant by "four pipelines"? Does the applicant mean four processors or does the applicant mean four pipeline queues?

Referring to **Claim 10**, the usage of "first stage" and "second stage" associated with a read cycle and "first instruction" and "second instruction" makes the claims indefinite because one of ordinary skill in the art at the time of the invention cannot assess the metes and bounds of the claims. What is meant by a "first stage", "second stage", "first instruction" and "second instruction"? A pipeline processor has a fetch step and read step. Does the first stage have both a fetch and a read in the same stage?

Referring to **Claim 17**, What is meant by a "plurality of stages"?

Referring to **Claim 20**, What is meant by a "data channel"?

Referring to **Claim 22** the usage of "first stage", "second stage", and " beginning a read cycle" makes the claims indefinite because one of ordinary skill in the art at the time of the invention cannot assess the metes and bounds of the claims. What is meant by a "first stage" and "second stage"? A pipeline processor has a fetch step and read step. Does the first stage have read cycle and does the second stage also have a read cycle?

Referring to **Claim 27**, the usage of "first stage", "second stage", and " beginning a read cycle" makes the claims indefinite because one of ordinary skill in the art at the time of the invention cannot assess the metes and bounds of the claims. What is meant by a "first stage" and "second stage"? A pipeline processor has a fetch step and read step. Does the first stage have read cycle and does the second stage also have a read cycle?

Referring to **Claim 30**, the applicant refers to a "double pipeline unit". What is meant by a "double pipeline unit"?

Referring to **Claim 32**, the applicant refers to a "quad pipeline unit"? What is meant by a "quad pipeline unit"?

Referring to **Claims 23-26**, these claims are indefinite because they never refer to an independent claims.

Referring to **Claims 29-31**, these claims are indefinite also because they never refer to an independent claim.

Double Patenting

12.0 The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

13.0 **Claims 1-9 & 14-21** are rejected under the judicially created doctrine of double patenting over **claims 1-9 & 12-18** of U. S. Patent No. 6,198,751 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

Referring to **Claim 1,** Claim 1 of U.S. patent No.; 6,198,751 teaches all of the limitation of the application **Claim 1**: a translator, input memory, info source, output memory and first protocol with a header and second protocol with a header. The application does not call for different headers for each protocol but requires different protocols. It would have been obvious to one of ordinary skill in the art at the time of the invention that different headers would mean different protocols are utilized.
In Addition: Claims 2-9 of the application are identical with Claims 2-9 of Patent No.: 6,198,751.

Referring to **Claim 14**, Claim 12 of the U.S. Patent No.: 6,198,751 teaches all of the limitations of claim 14 of the application including: translating loading microcode instruction set, loading at least a header into memory , providing info, providing output memory and performing sequentially, the application. The application does not expressly require loading microcode but requires loading instruction set or loading at least a header but requires loading a packet. It would have been obvious to one of ordinary skill in the art at the time of the that loading a header and loading microcode performs the same function of loading at least a header and loading an instruction set.
In Addition: claims 13-18 of the Patent are identical to claims 16-21 of the application.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claim Objections

14.0 **Claims 12-13** are objected to because of the following informalities: Referring to Claim 12, the examiner objects to the usage of the word "a" in the phrase "selecting a one of the sets.." per Pg 32 line 18 . The examiner recommends deleting the word "a".
Claim 13 is objected to because it depends upon claim 12. Appropriate correction is required.

Conclusion

15.0 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert W Wilson whose telephone number is 571/272-3075. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on 571/272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert W. Wilson

Robert W Wilson
Examiner
Art Unit 2661

RWW
September 27, 2004

KENNETH VANDERPUYE
PRIMARY EXAMINER